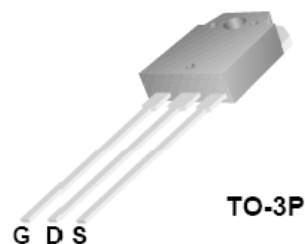


600V N-Channel MOSFET

General Description

This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.



Features

20A, 600V, $R_{DS(on)typ.} = 0.35\Omega @ V_{GS} = 10V$

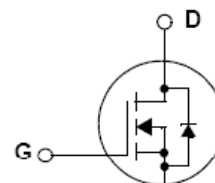
Low gate charge (50nC)

High ruggedness

Fast switching

100% avalanche tested

Improved dv/dt capability



Absolute Maximum Ratings T_c = 25 °C unless otherwise noted

Symbol	Parameter	JFAM20N60C	Units
V _{DSS}	Drain – Source Voltage	600	V
I _D	Drain Current	Continuous (T _c = 25 °C)	20*
		Continuous (T _c = 100 °C)	12.5*
I _{DM}	Drain Current - Pulsed (Note 1)	60	A
V _{GSS}	Gate – Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	450	mJ
I _{AR}	Avalanche Current (Note 1)	20	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	20.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	50	V/ns
P _D	Power Dissipation (T _c = 25 °C) -Derate above 25 °C	272	W
		2.17	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes 1/8" from case for 5 seconds	300	°C

*Drain current limited by maximum junction temperature.

Thermal characteristics

Symbol	Parameter	JFAM20N60C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.46	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics $T_c = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain – Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.5	--	$\text{V}/^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 480\text{ V}, T_c = 125^{\circ}\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source on-Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	--	0.35	0.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 10\text{ A}$ (Note 4)	--	18	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	2310	--	pF
C_{oss}	Output Capacitance		--	1270	--	pF
C_{rss}	Reverse Transfer Capacitance		--	85	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 300\text{ V}, I_D = 20.0\text{ A}, R_G = 25\ \Omega, V_{GS} = 10\text{ V}$ (Note 4,5)	--	60	--	ns
t_r	Turn-On Rise Time		--	130	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	220	--	ns
t_f	Turn-Off Fall Time		--	70	--	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 20.0\text{ A}, V_{GS} = 10\text{ V}$ (Note 4,5)	--	50	--	nC
Q_{gs}	Gate-Source Charge		--	15	--	nC
Q_{gd}	Gate-Drain Charge		--	23	--	nC
Drain – Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	80	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 20.0\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 20.0\text{ A}$	--	460	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	5.1	--	μC

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature
2. $L = 5.0\text{mH}$, $I_{AS} = 20\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$
3. $I_{SD} \leq 20.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$
4. Pulsed Test : Pulsed width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

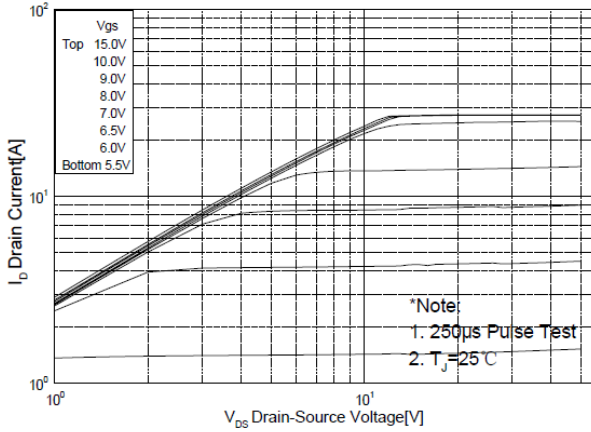


Figure 1. On-Region Characteristics

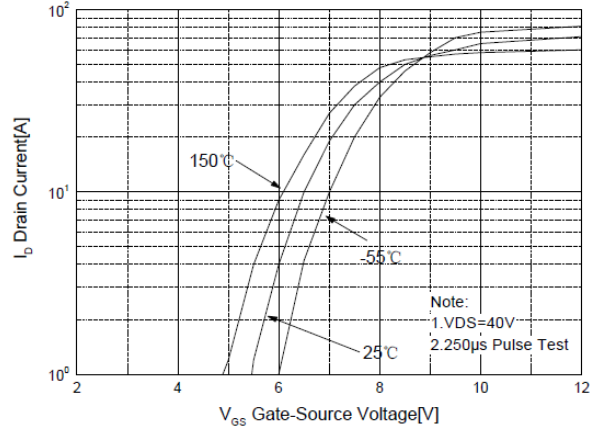


Figure 2. Transfer Characteristics

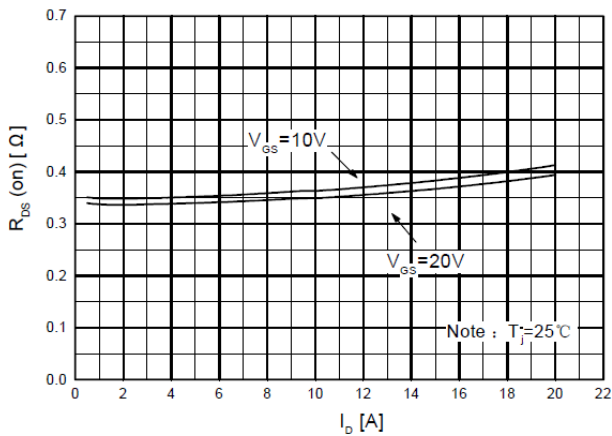


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

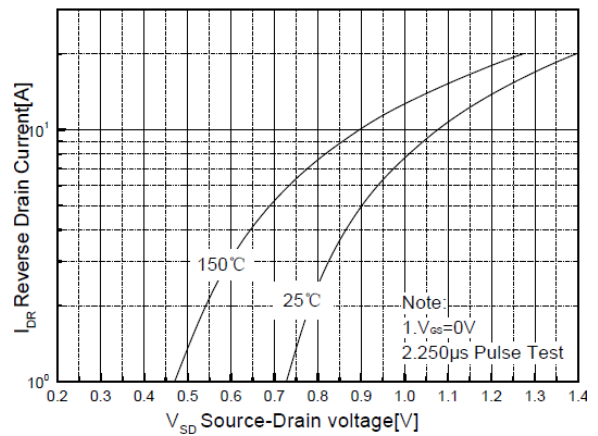


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

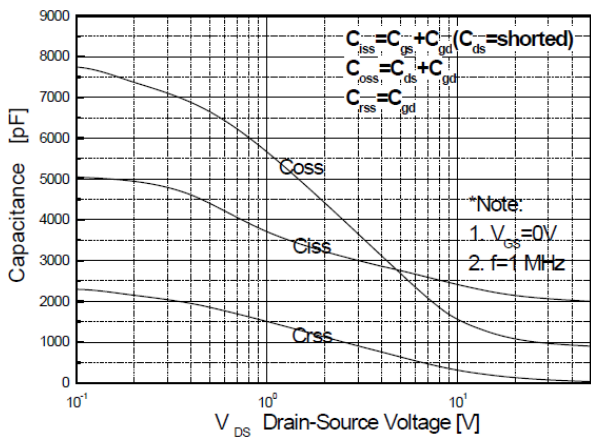


Figure 5. Capacitance Characteristics

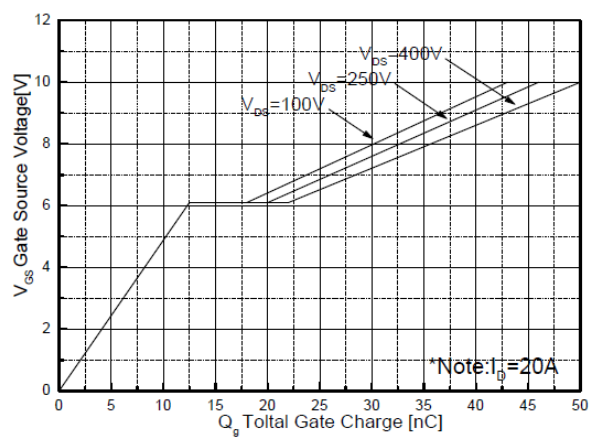


Figure 6. Gate Charge Characteristics

Typical Characteristics

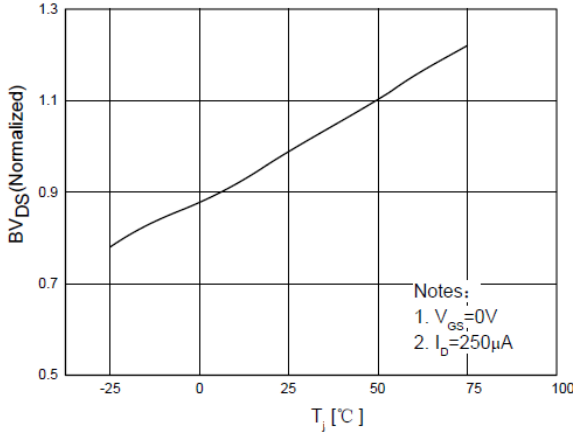


Figure 7. Breakdown Voltage Variation vs Temperature

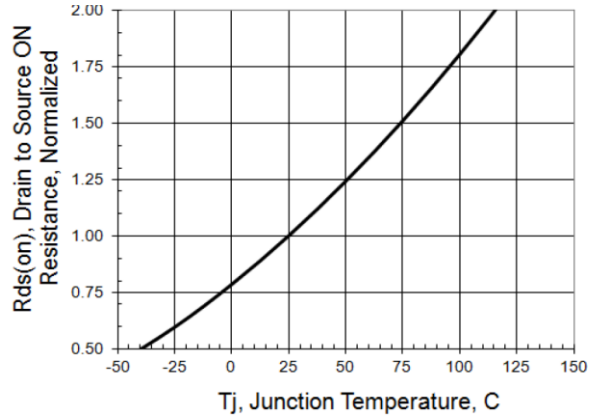


Figure 8. On-Resistance Variation vs Temperature

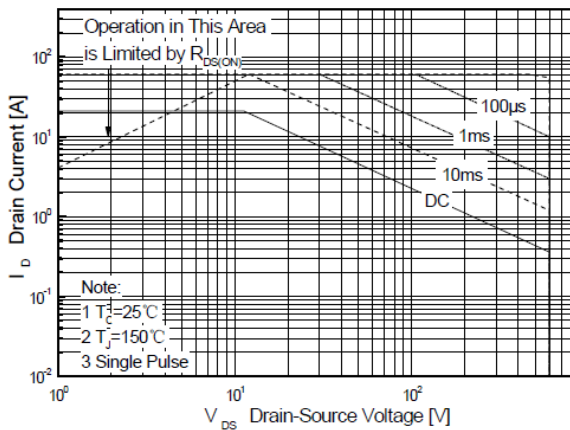


Figure 9-2. Maximum Safe Operating Area for JFAM20N60C

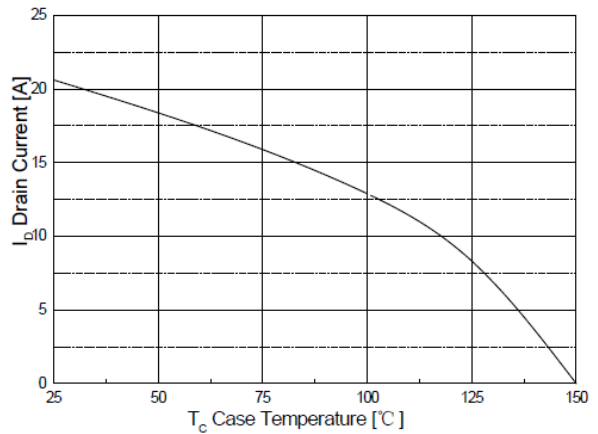


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics

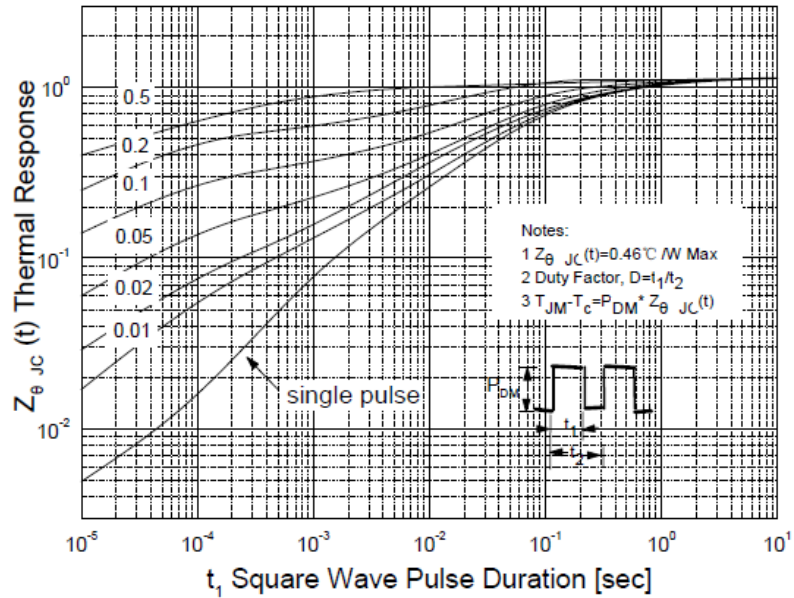
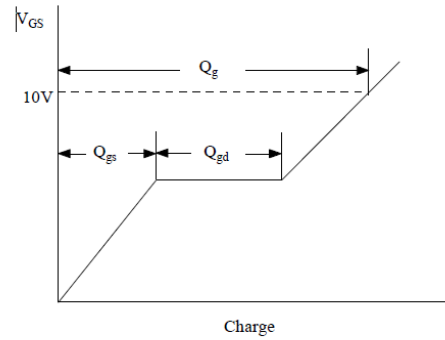
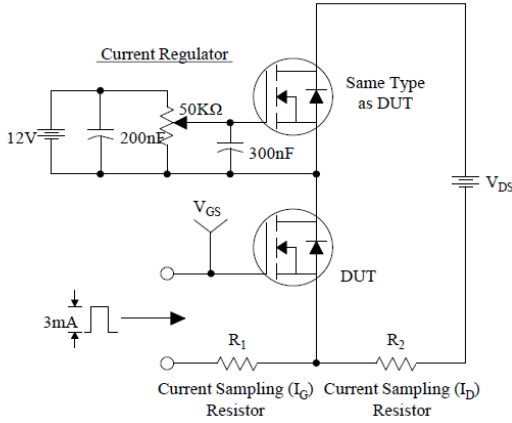
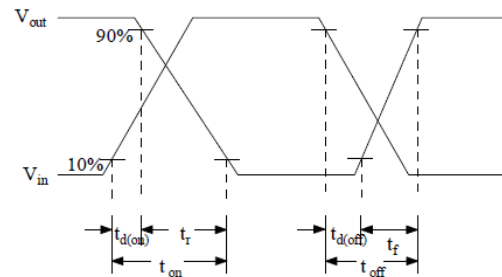
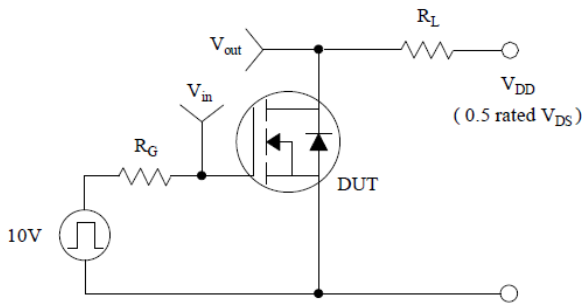


Figure 11-2. Transient Thermal Response Curve for JFAM20N60C

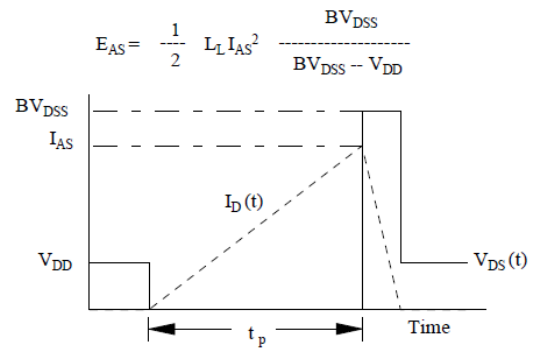
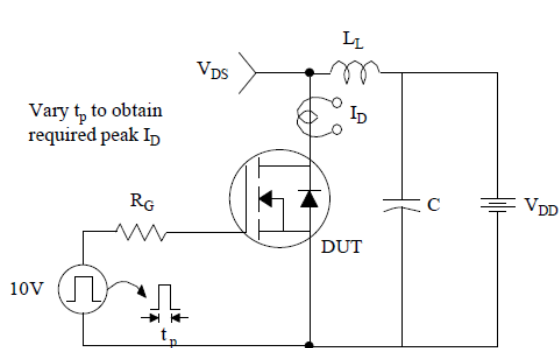
Test Circuit & Waveform



Gate Charge Test Circuit & Waveform

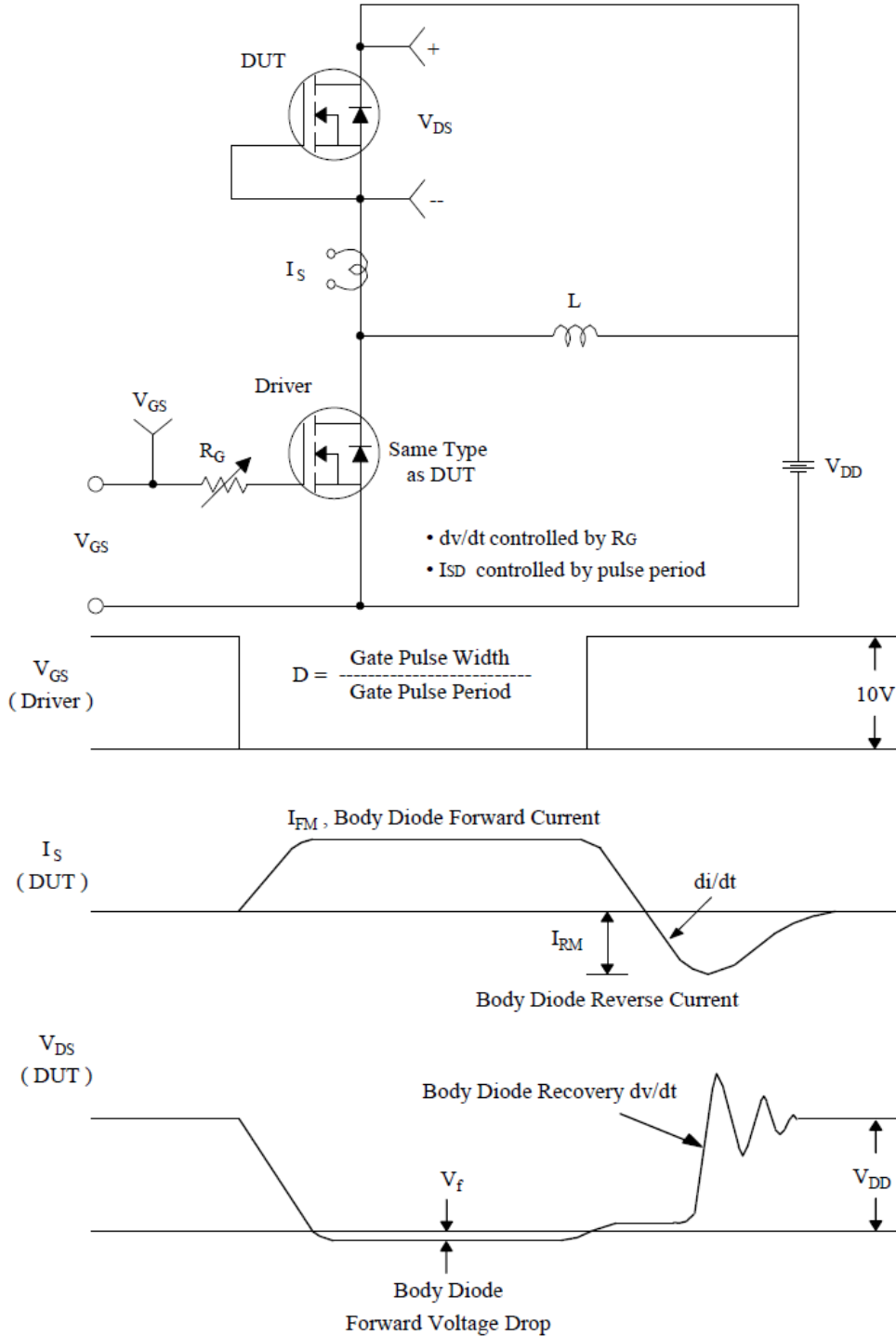


Resistive Switching Test Circuit & Waveforms



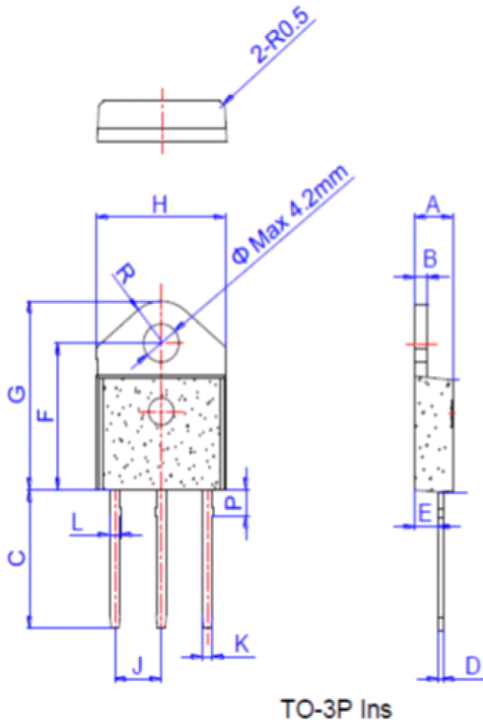
Unclamped Inductive Switching Test Circuit & Waveforms

Test Circuit & Waveform



Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-3P-3L-II PACKAGE OUTLINE



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.50		0.70	0.020		0.028
E	2.70		2.90	0.106		0.114
F	15.80		16.50	0.622		0.650
G	20.40		21.10	0.803		0.831
H	15.10		15.50	0.594		0.610
J	5.40		5.65	0.213		0.222
K	1.10		1.40	0.043		0.055
L	1.35		1.50	0.053		0.059
P	2.80		3.00	0.110		0.118
R		4.35			0.171	

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